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Upgrade Your Lab

Bipolar Transistor Amplifier Designing

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1. Introduction

The designing, building, measurement and analysis of amplifier circuits is an important laboratory experiment in undergraduate programme. As part of this course, students will learn to design amplifier circuits to achieve the required functionality using passive components (like resistors, capacitors etc.) and active components(like transistors, Op-Amps, etc.).

In this paper we have explained the basic theory and the various steps involved in the designing of amplifiers using bipolar transistors. For constructing an amplifier, we need transistor, resistors, capacitors and power supply/voltage source. For analysis purpose we need Digital Multimeter, Oscilloscopes, Function generators etc.

For learning and practising purpose it is always advisable to use breadboards to wire up the circuit instead of the soldering method, because it is easy to assemble, test and modify. We can also reuse the components and reduce wastage.

Any voltage source(Battery/Power supply) that we use in lab is having some internal resistance. So when we connect this supply in a circuit, there will be a voltage drop across its internal resistance and the actual voltage available to our circuit will be less. When more current is drawn from the battery the drop across internal resistance also will be more and the voltage available for the circuit will be less. That means, in order to get the full voltage of the source available for the circuit, the internal resistance of the voltage source should be ideally zero. In that case irrespective of the amount of current drawn by the circuit the voltage available for the circuit will remain the same. So we have to use a regulated power supply where the effective internal resistance is close to zero or close to ideal. In the case of unregulated power supply the available voltage will vary depending on the current drawn by the circuit.

2. Transistor as an Amplifier

- What is amplification?
  Amplification is the process of raising the strength of a signal without changing its frequency or shape. Amplification can be that of voltage signal or current signal. For amplification to take place the output signal should vary proportional to the input

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signal. If the variation is not in accordance with the input, then the output wave will be distorted or deformed and the amplification will not be faithful.

- How to get faithful amplification?
  We have seen that for faithful amplification, the output voltage/current should vary in accordance with the input signal. For this to happen, the transistor circuit is so designed that, the emitter-base junction is properly forward biased and collector-base junction is properly reverse biased. In this situation

$$I_E = I_C + I_B \tag{1}$$

  which means, collector current I_C will be very nearly equal to emitter current I_E and all the variations in the emitter current will be followed by the collector current .

Transistor can be used as an amplifier in three different configurations.

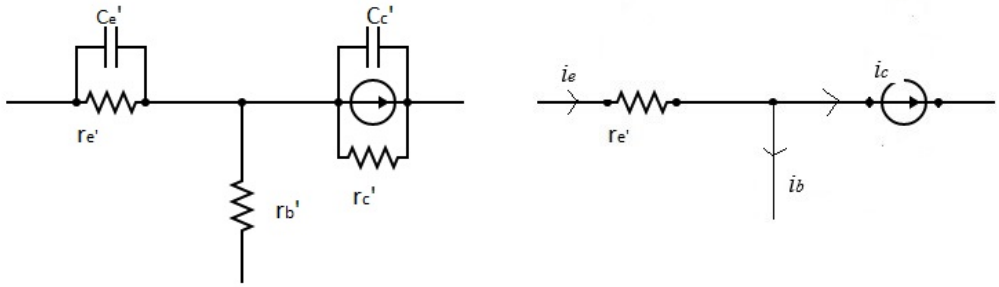
- Common Emitter(CE) configuration.
- Common Base(CB) configuration
- Common Collector(CC) configuration

For all three configurations, the emitter junction is always to be forward biased and the collector junction is to be reverse biased. Out of these, CE configuration is widely used for amplification purpose due to its high current gain, moderate voltage gain and better impedance matching. For CE configuration the emitter current is given by the relation,

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \tag{2}$$

where β (hybrid parameter h_{fe}) is the current amplification in CE configuration and I_{CBO} is the collector-base leakage current when emitter is open.

2.1. AC equivalent circuit—Usually while designing a transistor amplifier circuit, the various parameters like voltage, current and resistance values are fixed with the help of equivalent circuits. Since we are interested in ac amplification we need an ac equivalent circuit. Using this we can also analyse the voltage gain, power gain, input impedance and output impedance of the circuit. The equivalent circuit is shown in Fig: 1a.



(a) Equivalent circuit (b) Simplified equivalent circuit

Fig. 1. Transistor equivalent circuit

Here,
$C_e^{'}$ is emitter junction capacitance
$r_e^{'}$ is ac emitter resistance and
$r_b^{'}$ is ac base resistance
$C_c^{'}$ is collector junction capacitance

& $r_c^{'}$ is ac collector resistance.

The effect of $C_e^{'}$ and $C_c^{'}$ in the circuit operation can be neglected at ordinary signal frequencies. $r_b{}^{'} << r_e^{'}$ and is neglected. Since the collector junction is reverse biased, the junction resistance $r_c^{'}$ is very high of the order of MΩ. Therefore this parallel resistance can be considered as open.

Thus the above shown equivalent circuits can be simplified for practical purposes as shown in Fig:1b.This circuit is also referred as T-circuit.

$r_e^{'} = \frac{dV}{dI}$, where V is the junction voltage and I is the current through the junction. As per Shockley relation describing pn junction V-I characteristic,

$$I = I_s(e^{\frac{V}{kT/q}} - 1) \tag{3}$$

Here, I_s represents the reverse saturation current, k is Boltzmann constant, T is the room temperature in Kelvin and q is the electronic charge. The term kT/q represents the mean thermal energy of charge carriers and is called the Voltage equivalent of thermal energy(V_T).

$$V_T = \frac{kT}{q} = \frac{T}{11600} \tag{4}$$

ac dynamic resistance of emitter junction is,

$$\begin{aligned} r_e' &= \frac{1}{dI/dV} \\ \frac{dI}{dV} &= \frac{d}{dV}\left[I_s e^{V/V_T} - I_s\right] \\ &= \frac{I_s e^{V/V_T}}{V_T} \\ &= \frac{I + I_s}{V_T} \approx \frac{I}{V_T} \\ \therefore r_e' &= \frac{V_T}{I} = \frac{T}{11600 \times I} \end{aligned}$$

If the room temperature is taken as 300 K, and the junction current is replaced by emitter current, we get,

$$r_e' = \frac{26(mV)}{I_E(mA)} \tag{5}$$

2.2. Transistor characteristic—For CE configuration the output characteristic represents the relation between V_{CE} and I_C for various I_B values(Fig:2). The nature of this characteristic is relevant in the proper designing of amplifier circuits. In the output characteristic of a transistor, we can identify three different regions - saturation region, active region and cut off region.[1]

(1) **Saturation region:** In the saturation region(shaded in blue) the collector emitter voltage(V_{CE}) is very small and the CE junction is not reverse biased or the output current does not vary in accordance with the input current. This region should be avoided for amplification purpose. Below is given the collector-emitter voltage and base-emitter voltage corresponding to the saturation condition.

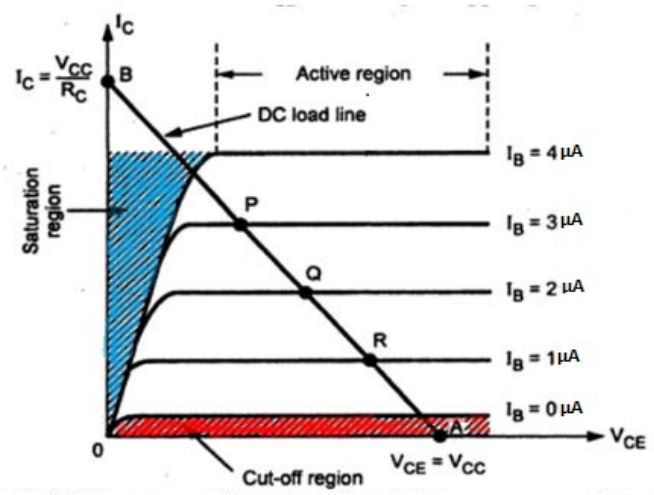


Fig. 2. CE output characteristic with dc load line

$$\left.\begin{aligned} V_{CE\,(sat)} &= 0.2V \\ V_{BE\,(sat)} &= 0.7V \end{aligned}\right\} \text{Si} \tag{6}$$

$$\left.\begin{aligned} V_{CE\,(sat)} &= 0.1V \\ V_{BE\,(sat)} &= 0.3V \end{aligned}\right\} \text{Ge} \tag{7}$$

If V_{CE} is less than this saturation voltage, transistor cannot function as an amplifier.

(2) **Cut off region :** The region below $I_B = 0$ curve is referred as cut off region (shaded in red). In this region both emitter and collector junctions are reverse biased and is not suitable for amplification purpose.

(3) **Active region:** The region on the right side of saturation region and above $I_B = 0$ curve in the output characteristic is known as active region. In this region emitter junction is forward biased and collector junction is reverse biased. Transistor amplifier is always designed to work in this region. In the active region you will see that the output current I_C is changing in accordance with the input currentI_B and that is the primary requirement for faithful amplification.

2.3. Biasing of Transistors—Usually the signals that we amplify are ac signals of different frequencies. These signals are superimposed on the dc condition prevailing in the circuit. So the first step while designing an amplifier circuit is to fix the dc base, emitter and collector current and dc voltages across the three terminals of transistor. ie.we have to fix the operating point or the Q point(Quiescent point). The Q point or the operating point represents the values of V_{CE} & I_C when no input signal is applied. The operating point should be chosen in such a way that, for all instances of the input signal the output remain in the active region.

- Base emitter junction must always be forward biased. If you are using a silicon transistor, this voltage should be around 0.6 - 0.7 Volt.
- Collector base junction must always be reverse biased.

What is the purpose of biasing?

We have already discussed that, the emitter junction must be forward biased and collector junction must be reverse biased for amplification action. In other words, transistor should be operated in the active region to work as an amplifier. This is achieved using a suitable biasing circuit.

How to provide biasing?

The biasing is done with the help of suitable supporting circuitry. To understand the designing of circuit elements we should look into the two important concepts- operating point and load line. In the simple circuit shown in Fig:3, there is no signal given at the input. That means only DC prevails in the circuit. Applying Kirchoff's law to the collector side we get,

$$V_{CC} = I_C R_C + V_{CE}$$
$$\therefore I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \tag{8}$$

Now we will consider two extreme cases.

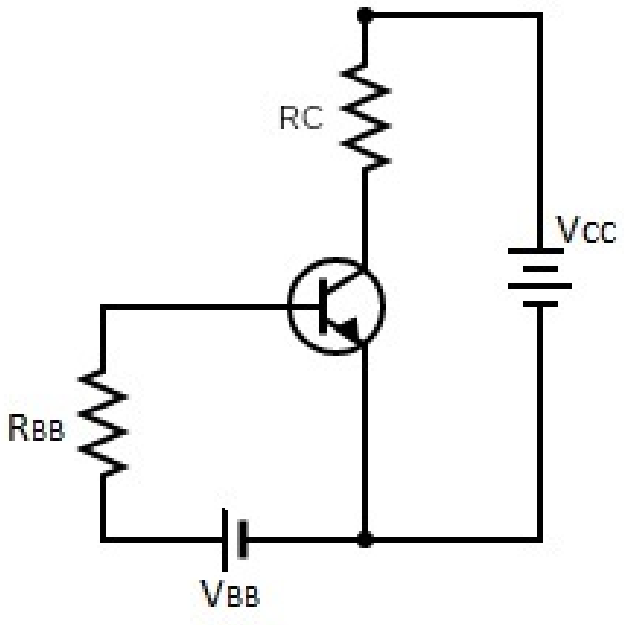


Fig. 3. Basic amplifier circuit

(1) When the collector current $I_C = 0$, Collector emitter voltage V_{CE} is $V_{CE_{max}} = V_{CC}$ This gives the cut-off point A in the output graph shown in Fig:2.

(2) When collector emitter voltage $V_{CE_{max}=0}$, collector current is maximum, and I_{Cmax} $=\frac{V_{CC}}{R_C}$ and this gives point B in the output graph shown in Fig:2.

If we mark these two points on the $V_{CE} - I_C$ graph, and join them we get a straight line. This line is representing the DC load line where the slope is decided by the value of R_C. The V_{CE} & I_C values corresponding to Q point are represented as V_{CEQ} & I_{CQ} respectively. The applied input signal will be superimposed over this Q point and the V_{CE} & I_C values changes about this Q point. If the Q point is chosen closer to the saturation or cut off region, there is always a chance for the output signal to be distorted. So while designing transistor amplifiers, it is always ideal to fix the operating point on the load line, mid-way between the

saturation and cut-off points.

2.4. Factors affecting transistor parameters—There are many external factors that influence transistor parameters resulting in variation in transistor performance. For example,

- The current amplification β changes with temperature, aging or device variation.
- collector current I_C varies with temperature.
- Base emitter voltage V_{BE} varies with temperature because the resistivity of semiconductor decreases with rise in temperature and so the voltage drop across base emitter junction also falls. V_{BE} falls roughly by 2V for every 10^0C rise in temperature.

Due to the above mentioned factors there is always a chance for the output signal to be distorted. So, while designing transistor amplifiers, it is always ideal to fix the operating point on the load line, mid-way between the saturation and cut-off points to allow maximum voltage swing of output signal on either side of reference voltage.

2.5. Stability factor—The inherent variations in the transistor parameters due to temperature changes, aging or transistor replacements may result in shift in the operating point. This causes distortion in the output signal. So we have to make the operating point stable or independent of temperature changes or variations in transistor parameters like I_{CBO}, β or V_{BE}. This can be ensured by optimising the stability factor of the circuit.Stability factor(S) for the transistor amplifier circuit can be measured in terms of the change in I_C with change in I_{CBO}, β or V_{BE} . Thus, stability factor S can be represented as,

$$S = \left.\frac{\partial I_c}{\partial I_{CBO}}\right|_{\beta} \tag{9}$$

OR

$$S' = \left.\frac{\partial I_c}{\partial \beta}\right|_{I_{CBO}} \tag{10}$$

OR

$$S'' = \left.\frac{\partial I_c}{\partial V_{BE}}\right|_{I_{CBO}} \tag{11}$$

If we optimize stability factor against any one kind of these three variations, then automatically the circuit will be stable or the Q-point will not be shifted with the other kind of variations also. One way of getting the expression for stability factor is by differentiating equation:2 with respect to I_C.Thus,

$$\begin{aligned} 1 &= \beta \frac{\partial I_B}{\partial I_C} + (\beta+1)\frac{\partial I_{CBO}}{\partial I_C} \\ 1 &= \beta \frac{\partial I_B}{\partial I_C} + \frac{(\beta+1)}{S} \\ S &= \frac{(\beta+1)}{1-\beta\frac{\partial I_B}{\partial I_C}} \end{aligned} \tag{12}$$

The value of S is to be maintained below 25 for good performance.

3. Transistor Biasing Techniques

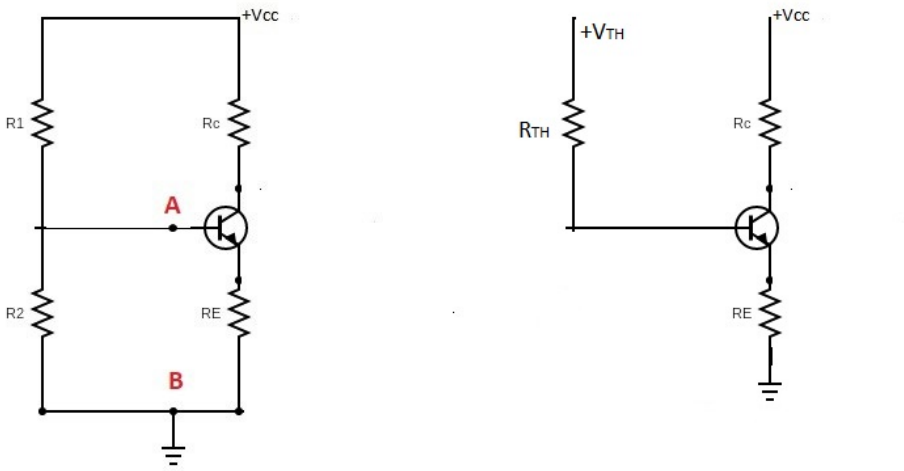
There are various methods of biasing a transistor. Any biasing circuit should maintain the transistor in the active region and also should ensure stability of operating point(Q-point). Different methods used for providing bias for transistor are,

(1) Fixed bias or Base bias:
In this method circuit stabilization is very poor or stability factor S is very high and the Q-point shifts drastically with change in temperature. Therefore fixed bias is almost never used in transistor circuits even though the designing is very simple.

(2) Self bias or Biasing with emitter feedback resistor:
This technique provides good circuit stability against changes in β, *.e.* $I_C \neq f(\beta)$. This is achieved with the help of emitter feed back resistor.

(3) Self bias with Voltage divider circuit:
This is the most widely used biasing method (Fig:4a). Using Thevenin's theorem we can redraw the circuit as in Fig:4b. Here Thevenized voltage V_{Th} is in series with thevenized resistance R_{TH}. V_{Th} is the open circuit voltage between $A\&B$

$$V_{Th} = \frac{V_{CC}R_2}{R_1 + R_2} \tag{13}$$



(a) Bias circuit (b) Thevenized circuit

Fig. 4. Voltage divider bias

Thevenized resistance is obtained by finding the equivalent resistance between A & B after short circuiting the voltage source. Thus, R_1 R_2 are parallel and so,

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} \tag{14}$$

. Applying Kirchoff's voltage law to the base side,

$$\begin{aligned} V_{Th} &= I_B R_{Th} + V_{BE} + I_E R_E \\ &= I_B R_{Th} + V_{BE} + I_C R_E \\ &= \frac{I_C}{\beta} R_{Th} + V_{BE} + I_C R_E \\ &= I_C[R_E + \frac{R_{Th}}{\beta}] + V_{BE} \end{aligned}$$

$$\therefore I_C = \frac{V_{Th} - V_{BE}}{(R_E + \frac{R_{Th}}{\beta})}$$

By making $R_E > \frac{R_{Th}}{\beta}$ above equation can be approximated as,

$$I_C = \frac{V_{Th} - V_{BE}}{R_E} \tag{15}$$

- Circuit provides very good stabilization. From eqn.15, we have,

$$V_{Th} = V_{BE} + I_C R_E \tag{16}$$

when I_C increases due to rise in temperature, $I_C R_E$ increases. We know that V_{Th} is independent of I_C. Therefore as per eqn.16, V_{BE} reduces and correspondingly I_B decreases. The reduction in I_B leads to corresponding reduction in I_C . This brings back the I_C to the original value itself.

4. Design Procedure

(1) Selection of operating point

(1) First step in the design procedure is selection of operating point. For fixing the operating point, we have to draw the DC load line. Applying KVL to the collector emitter side. We have,
$V_{CC} = I_C R_C + I_E R_E + V_{CE}$. But $I_E \approx I_C$

$$\therefore V_{CC} = I_C(R_C + R_E) + V_{CE} \tag{17}$$

- When the collector current $I_C = 0$, Collector emitter voltage V_{CE} is $V_{CE_{max}} = V_{CC}$ This gives the cut-off point A in the output graph.
- When collector emitter voltage $V_{CE} = 0$, collector current is maximum, and $I_{Cmax} = \frac{V_{CC}}{(R_C + R_E)}$. This gives the saturation point B on the graph.

If we mark these two points on the $V_{CE} - I_C$ graph, and join them we get a straight line. This line is representing the DC load line. Now we have to mark the values corresponding to Q point, V_{CEQ} & I_{CQ}. Usually the operating point is to be selected near the middle of the load line.

(2) However in most of the situations the characteristic curve may not be available. In that case it is always safe to make

$$V_{CEQ} = \frac{1}{2} V_{CC} \tag{18}$$

so that the output voltage can have maximum swing in both positive and negative directions about the operating point.
The optimum value of I_{CQ} can be selected from the data sheet as the bias current at which h_{fe} is measured. For BC 107 (which is a silicon planar npn transistor, used in low noise - general purpose audio amplifier circuits) it is given as $2\ mA$. and for CL 100 (which is a medium power silicon planar transistor) it is given as $150\ mA$.

(2) Fixing the resistor values

(1) Resistors R_C & R_E

The stability of the circuit against the variation in temperature is improved with higher values of R_E. But larger values of R_E reduces the voltage drop across R_C and thereby reduces the output voltage swing. So as a general thumb rule, R_E is so selected to have a voltage drop of $10\ \%$ of V_{CC} across it. That is,

$$V_{R_E} = 0.1 \times V_{CC} \tag{19}$$

$$\therefore R_E = \frac{V_{R_E}}{I_E} = 0.1 \times \frac{V_{CC}}{I_{CQ}} \tag{20}$$

Corresponding to the operating point, eqn.17, can be rewritten as,

$$V_{CC} = I_{CQ}R_C + I_{CQ}R_E + V_{CEQ} \tag{21}$$

As per eqn.18, $V_{CEQ} = 0.5 \times V_{CC}$
and as per eqn.20 $V_{R_E} = I_{CQ}R_E = 0.1 \times V_{CC}$
So the remaining voltage, will drop across R_C. Thus,

$$V_{R_C} = 0.4 \times V_{CC} \tag{22}$$

$$\therefore R_C = \frac{V_{RC}}{I_{CQ}} = 0.4 \times \frac{V_{CC}}{I_{CQ}} \tag{23}$$

(2) Resistors R_1 & R_2

The base current corresponding to Q point is obtained as,

$$I_{BQ} = \frac{I_{CQ}}{h_{fe}} \tag{24}$$

The current through R_1 must be at least equal to $10I_B$ for good stabilization.This is to minimize the loading problem at the input of amplifier. That is $I_1 \geq 10I_B$. This current branches into $I_2 = 9I_B$ through R_2 and I_B as base current. Applying KVL to the base -emitter circuit,

$$V_{R_2} = V_{BE} + V_{R_E} = 9I_BR_2 \tag{25}$$

V_{BE} we can get from data sheet, V_{R_E} can be obtained as per eqn.19, I_B is determined as per eqn. 24. Thus we get R_2.
Now R_1 is to be determined. For that, applying KVL,

$$V_{R_1} = 10I_{BQ}R_1 = V_{CC} - V_{R_2} \tag{26}$$

Using this equation we can calculate the value of R_2.

(3) Fixing the capacitor values

(1) Emitter bypass capacitor C_E

This capacitance should provide a low reactance path to the signal enabling it to bypass the signal current to ground and thereby reducing negative feed back. So its value is chosen in such a way as to bypass even the lowest frequency input signal . Thus as a general thumb rule the reactance of C_E is chosen as,

$$X_{C_E} = \frac{1}{2\pi f_{min} C_E} \leq \frac{R_E}{10} \tag{27}$$

From this relation, C_E is calculated(Usually a few tens of microfarad would be required).

(2) Coupling capacitors C_{in} & C_{out}

These capacitors should isolate dc and couple only the ac to the next stage. Thus we have two coupling capacitors, C_{in} & C_{out}. Using the equations given below we can determine these capacitances.

$$X_{C_{in}} = \frac{1}{2\pi f_{min} C_{in}} \leq \frac{R_{in}}{10} = \frac{1}{10}\left[R_1 \parallel R_2 \parallel h_{fe} r'_e\right] \tag{28}$$

Similarly,

$$X_{C_{out}} = \frac{1}{2\pi f_{min} C_{out}} \leq \frac{R_{out}}{10} = \frac{R_C}{10} \tag{29}$$

f_{min} in the above equations represent the lowest frequency of input signal. It should be noted that the lower cut-off frequency f_L of a transistor amplifier is determined by the combined effect of C_E, C_{in} & C_{out}

4.0.1. Example—As a practical example let us design circuit elements for an amplifier using BC 107. Using DMM let the measured value of h_{fe} = 250.

Let us take $V_{CC} = 10V$, and $I_{CQ} = 2mA$

(1) Resistors R_C & R_E

$I_E \approx I_{CQ}$
$V_{CEQ} = \frac{1}{2}V_{CC} = \frac{10}{2} = 5V$
$V_{R_E} = 0.1 \times V_{CC} = 0.1 \times 10 = 1V$

$\therefore R_E = \frac{V_{R_E}}{I_E} = \frac{1}{2\times10^{-3}} = 500\Omega$

$V_{R_C} = 0.4 \times V_{CC} = 0.4 \times 10 = 4V$

$\therefore R_C = \frac{V_{RC}}{I_{CQ}} = \frac{4}{2\times10^{-3}} = 2k\Omega$

(2) Resistors R_1 & R_2

$I_{BQ} = \frac{I_{CQ}}{h_{fe}} = \frac{2\times10^{-3}}{250} = 8\mu A$
$\mathrm{I}_1 \geq 10I_B = 10 \times 8 \times 10^{-6} = 80\mu A$

$V_{R_2} = 9I_{BQ}R_2 = V_{BE} + V_{R_E} = 0.6 + 1 = 1.6V$

$\therefore R_2 = \frac{V_{R_2}}{9I_{BQ}} = \frac{1.6}{9\times8\times10^{-6}} = 22.2k\Omega$

$V_{R_1} = I_1R_1 = V_{CC} - V_{R_2} = 10 - 1.6 = 8.4V$

$\therefore R_1 = \frac{8.4}{80\times10^{-6}} = 105k\Omega$

(3) Emitter bypass capacitor R_E

Let the lowest frequency to be amplified be, $f_{min} = 100Hz$

$X_{C_E} = \frac{1}{2\pi f_{min}C_E} = \frac{1}{2\pi\times100\times C_E}$

As per the designing rule, $\frac{1}{2\pi\times100\times C_E} \leq \frac{500}{10}$

$\therefore C_E \geq \frac{1}{2\pi\times100\times50} \geq 31.8\mu F$(Use $47\mu F$)

(4) Coupling capacitors C_{in} & C_{out}

$r'_e = \frac{26mV}{I_E(mA)} = \frac{26}{2} = 13\Omega$

$X_{C_{in}} = \frac{1}{2\pi\times100\times C_{in}}$

$\frac{R_{in}}{10} = \frac{1}{10}\left[R_1 \parallel R_2 \parallel h_{fe}r'_e\right] = 280\Omega$

$X_{C_{in}} \leq \frac{R_{in}}{10}$

$\frac{1}{2\pi\times100\times C_{in}} \leq 280\Omega$

$\therefore C_{in} \geq \frac{1}{2\pi\times100\times280} \geq 5.7\mu F$ (Use 10 μF)

$X_{C_{out}} = \frac{1}{2\pi\times100\times C_{out}} \leq \frac{R_C}{10} = \frac{2\times10^3}{10}$=200 Ω

$C_{out} \geq \frac{1}{2\pi\times100\times200} = 7.96\mu F \approx 10\mu F$

5. Procedure

Connect the circuit as shown in Fig:5 and study the performance.

5.1. Voltage and Power gain—Voltage gain is measured experimentally as,

$$A_V = \frac{V_{out}}{V_{in}} \tag{30}$$

Theoretical voltage gain of the amplifier is,

$$A_V = \frac{Z_{out}}{r'_e} \tag{31}$$

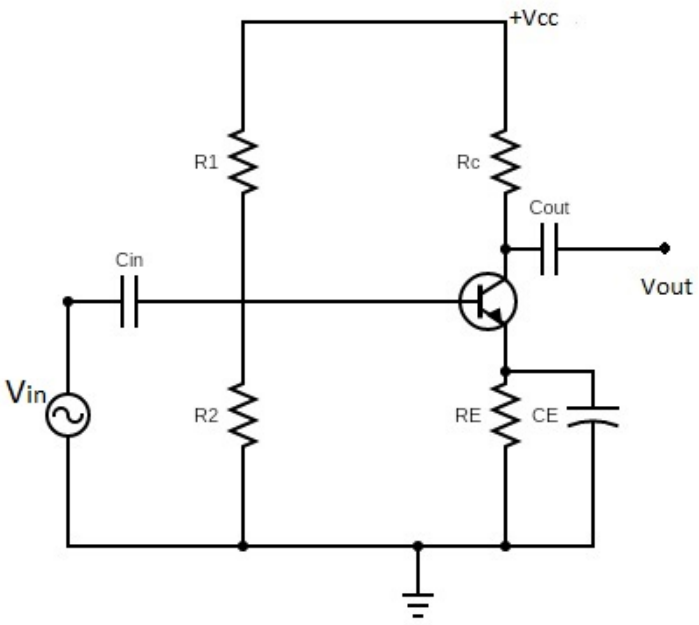


Fig. 5. Amplifier circuit

Power gain is calculated experimentally as,

$$A_P = (\frac{V_{out}}{V_{in}})^2 \frac{Zin}{Z_{out}} \tag{32}$$

5.2. Input and Output impedance—The input impedance Z_{in} of an amplifier is defined as the ratio of input signal voltage V_{in} and input signal current i_{in} flowing into the amplifier.

$$R_{in} = \frac{V_{in}}{i_{in}} \tag{33}$$

To measure i_{in}, a suitable Pot R_X is connected between points A and B as in Fig.6 Now measure the peak to peak voltage V_{AC} between points A & C and V_{BC} or V_{in} between B & C using an oscilloscope.[2]

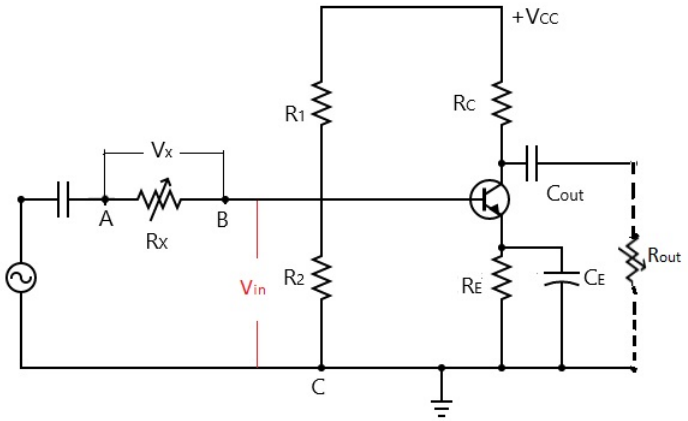


Fig. 6. Circuit to measure Input and output impedance

Now

$$Z_{in} = \frac{V_{BC}}{(V_{AC} - V_{BC})} \times R_X \tag{34}$$

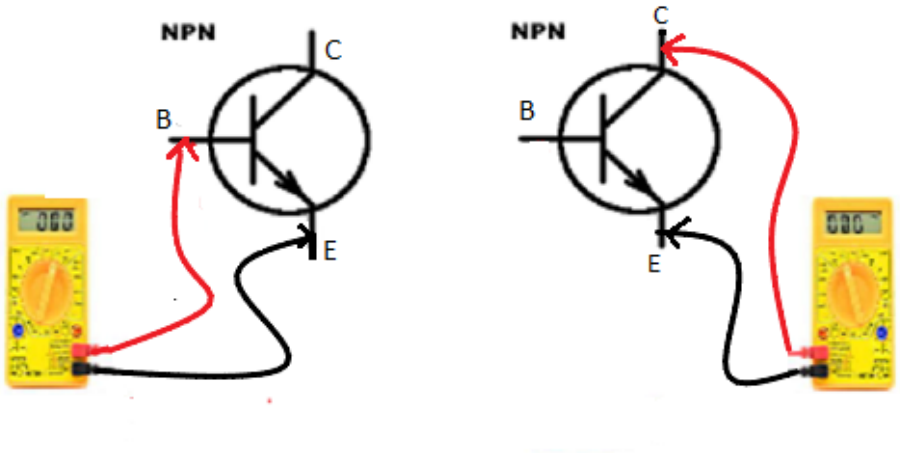
Theoretically input impedance is,

$$Z_{in} = R_1 \parallel R_2 \parallel \beta r'_e \tag{35}$$

The output impedance of the amplifierZ_{out} is determined experimentally . by connecting a pot R_{out} to the output circuit as shown in figure. Now the output signal peak to peak voltage is measured without R_{out}. Then connect R_{out} and it is adjusted until the output voltage becomes one half of the initial value. R_{out} is removed and its resistance is measured. This is equal to the output impedance Z_{out}. Theoretically,

$$Z_{out} = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L} \tag{36}$$

5.3. Trouble shooting—.[3] As we have mentioned earlier, we expect an amplified wave without distortion at the output. Suppose there is no output or we are getting a distorted output, we have to perform the following trouble shooting.



(a) Checking V_{BE} (b) Checking V_{CE}

Fig. 7. Checking the dc biasing

(1) Check the dc operation of the amplifier. For this the ac signal source is switched off and the dc voltages are to be measured.

(2) Measure the emitter base voltage V_{BE} as shown in Fig:7a.Remember that the red lead of DMM should be connected to the base terminal and the black lead to the emitter terminal for an npn transistor. The measured voltage should be sufficient enough to forward bias the emitter junction. V_{BE} ranges from 0.55 - 0.75 Volt for silicon transistor and if the measured value is not in this range the connection/designing should be checked.

(3) Measure the Collector-to-emitter voltage V_{CE} as shown in fig:7b. This should be above the saturation value for the transistor to be in the active region. As per the design, here we have taken $V_{CE} = \frac{V_{CC}}{2}$. Similarly measure the voltage across emitter resistance (V_{R_E}) and collector resistance (V_{R_C}). According to our design $V_{R_E} \approx 10\%$ V_{CC}, $V_{R_C} \approx 40\ \%\ V_{CC}$ .If the measured values are not near to these designed values, circuit is to be checked for BJT damage or wrong design.

Notes and References

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